



UNIVERSITY OF NAIROBI

SCHOOL OF ENGINEERING

**DEPARTMENT OF ELECTRICAL AND INFORMATION
ENGINEERING**

**DESIGN OF A MICROWAVE DOWNCONVERTER
PROJECT NUMBER: 84**

STUDENT NAME: OCHIENG ERICK OBWANDA.

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SUPERVISOR: MR. OMBURA.

EXAMINER: PROF. MANG'OLI

A project report submitted in partial fulfillment of the requirements for the award of the degree of BSc. Electrical and Electronics Engineering.

DECLARATION OF ORIGINALITY

NAME: Ochieng Erick Obwanda
REGISTRATION NUMBER: F17/2572/2010
COLLEGE: Architecture and Engineering
SCHOOL: Engineering
DEPARTMENT: Electrical and Information Engineering
COURSE: Bsc.in Electrical & Electronic Engineering
PROJECT NAME: Microwave Frequency Down Converter

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Acknowledgement

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CHAPTER1: INTRODUCTION

1.1OBJECTIVES

The goal of this design project is to design a microwave frequency down converter which operates at 1GHz.

1.2 GENERAL DESCRIPTION

A microwave frequency down converter is made of three main components:

1. Low noise amplifier which amplifies at the specific required frequency of operation which in this case is 1GHz.
2. An oscillator which produces an oscillatory signal to be used in the determination of the lower side band and the upper side band.
3. Mixer circuit which mixes the two signals to produce the lower side band frequency without or with minimal distortion of other wave properties such as phase angle.

CHAPTER 2 : LITERATURE REVIEW

2.1 LOW NOISE AMPLIFIER

Low noise amplifiers represent one of the basic building blocks of the communication system. The purpose of the LNA is to amplify the received signal to acceptable levels while minimizing the noise it adds.

The following are the design considerations:

1. Matching Impedances.

2. Power transfer.

3. Power consumption.

4. Noise.

5. Stability.

6. Linearity.

The first step involved the selection of the transistor for the amplifier. This is done based on the S-parameters of transistor and the noise figures given in the data sheet by the manufacturer of the transistor. The chosen transistor was FHX35LG. Its data sheet is as follows:

GHZ S MA R 50

! S-parameter data

0.0	0.0	0.0	0.0	0.0	0.0
0.0	0.0	0.0			
.100	.996	-3.5	4.576	177.2	.002
81.2	.516	-2.5			
.500	.994	-12.1	4.548	169.0	.012
79.3	.517	-10.2			
1.000	.982	-23.5	4.471	158.5	.023
73.1	.513	-19.9			
2.000	.950	-44.7	4.304	139.3	.043
57.9	.498	-38.0			
3.000	.912	-64.6	4.026	121.0	.059
44.6	.483	-54.9			

4.000	.867	-84.0	3.742	103.1	.071	
31.8	.462	-71.9				
5.000	.821	-101.6	3.436	86.6	.079	
20.0	.446	-87.6				
6.000	.783	-117.5	3.132	71.6	.085	
9.8	.439	-102.2				
7.000	.757	-130.9	2.881	57.9	.087	
0.9	.441	-115.3				
8.000	.738	-142.8	2.659	45.0	.088	-
7.1	.452	-126.7				
9.000	.726	-153.8	2.497	32.4	.090	-
15.3	.468	-136.9				
10.000	.707	-164.5	2.347	20.2	.092	-
21.7	.480	-146.1				
11.000	.680	-174.1	2.206	8.4	.090	-
27.8	.494	-156.0				

12.000	.654	176.1	2.101	-3.4	.090	-
35.5	.503	-164.8				

13.000	.638	166.0	2.035	-15.1	.091	-
42.6	.514	-173.8				

14.000	.626	157.1	2.003	-26.2	.093	-
49.6	.537	178.4				

15.000	.607	147.8	1.975	-37.6	.094	-
55.8	.559	171.0				

16.000	.565	138.4	1.917	-50.1	.097	-
64.7	.564	162.7				

17.000	.528	127.2	1.924	-62.9	.102	-
73.3	.567	154.4				

18.000	.484	112.8	1.966	-77.1	.109	-
86.2	.572	142.7				

19.000	.421	93.5	1.932	-91.7	.116	-
96.2	.581	113.1				

20.000 .380 74.2 1.991 -107.4 .127 -
110.9 .547 124.3

! Noise data 4/90

0.5 1.6 .41 32.0 .71

1.0 1.4 .38 72.0 .16

1.5 1.6 .26 141.0 .30

2 1.40 .81 32.0 .58

4 1.90 .74 63.0 .42

6 1.68 .69 93.0 .30

8 2.86 .64 127.0 .20

10 2.03 .60 148.0 .12

12 2.20 .56 175.0 .08

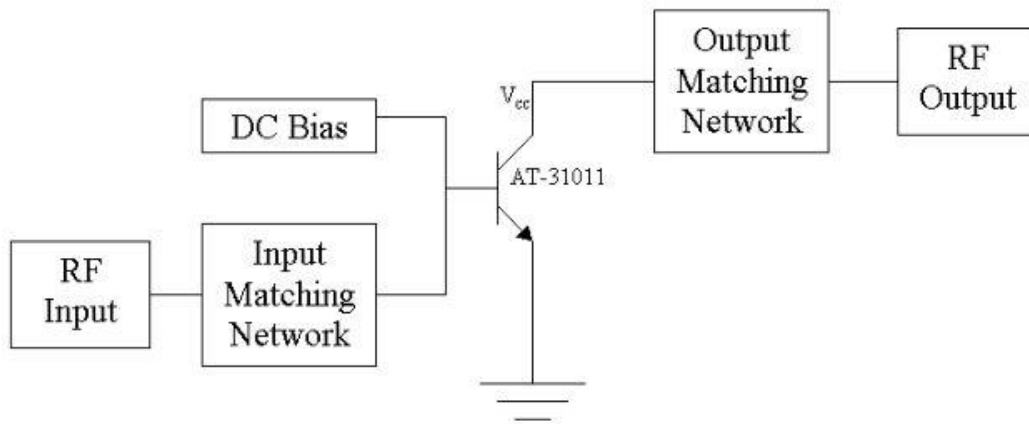
14 2.38 .53 -162.0 .08

16 2.54 .50 -139.0 .10

18 2.70 .48 -117.0 .14

The figure below shows the block diagram of an amplifier circuit:

Figure 1. Circuit Layout



2.1.1 INPUT MATCHING NETWORK

This is done so as to achieve maximum power transfer in the input section of the transistor. This is because it eliminates reflections in the input stage.

$$\Gamma = \frac{z - 1}{z + 1}$$

This is the expression for reflection coefficient. This property of an transistor is further illustrated by the S11 parameter of the transistor. This parameter helps establish the matching impedance:

$$Z_{in} = Z_o S_{11} + 1/1 - S_{11}$$

From the given parameters the calc input impedance are as follows:

$$0.982\text{Ang}-23.5 + 1/1 - 0.982\text{Ang} -23.5$$

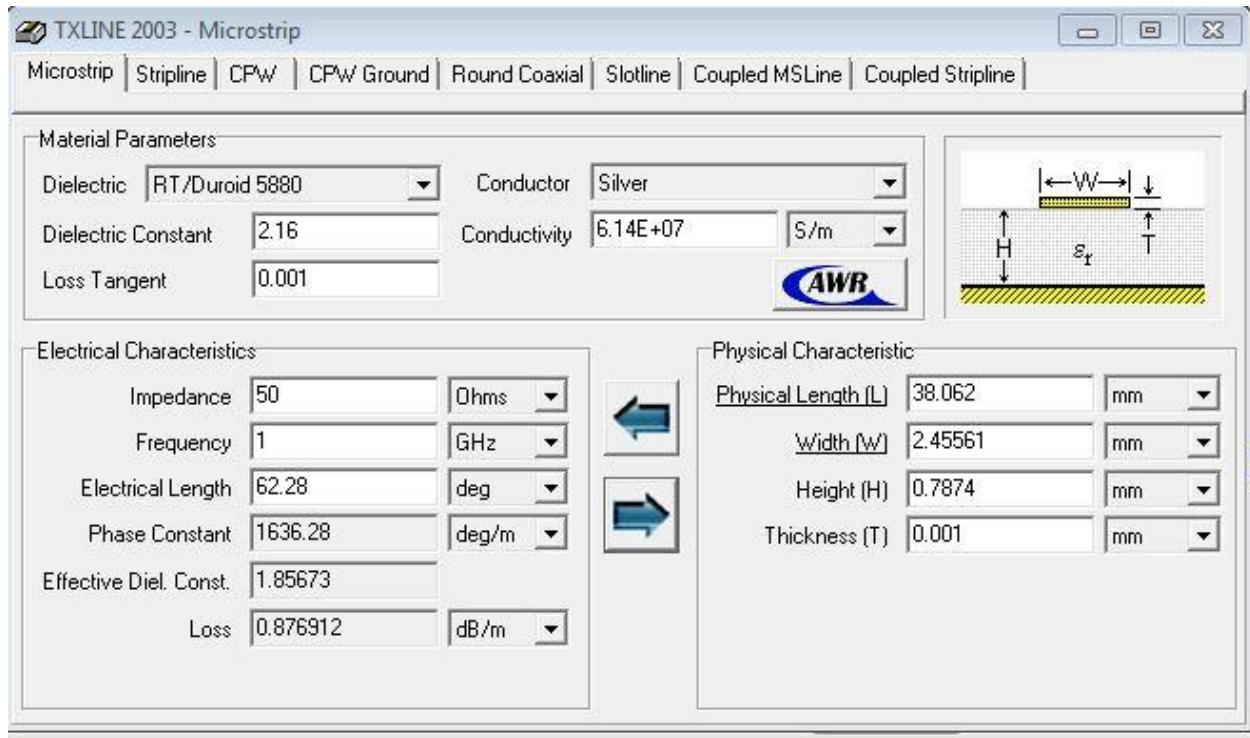
$$=4.8029\text{Ang}-87.$$

Using the single stub matching method the input matching network was constructed from the Smith chart.

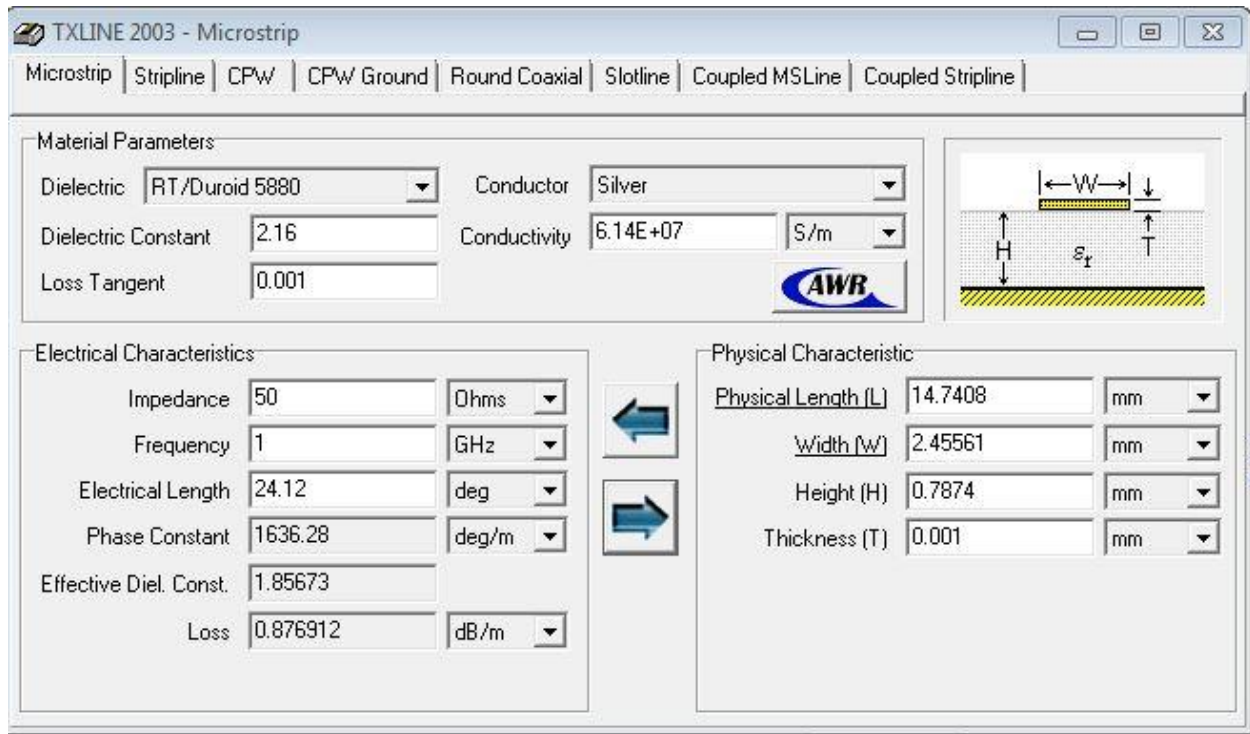
In single-stub tuning the two adjustable parameters are the distance, d , from the load to the stub position, and the value of susceptance or reactance provided by the stub. For the shunt-stub case, the basic idea is to select d so that the admittance, Y , seen looking into the line at a distance d from the load is of the form $Y_0 + jB$. Then the stub susceptance is chosen as $-jB$, resulting in a matched condition. For the series-stub case, the distance d is selected so that the impedance, Z , seen looking into the line at a distance d from the load is of the form $Z_0 + jX$. Then the stub reactance is chosen as $-jX$, resulting in a matched condition. The attached smith chart shows the matching process.

The attained results are fed into the AWR TX tool to find the actual physical properties of the line.

The TX tool is fed the impedance got and the desired dielectric is selected for the microstrip to be used in the circuit simulation. The tool calculates the width of the line and the length at the desired operating frequency. This is as shown by the caption shown below:



The stub calculations are as follows:



The above calculations were used as input matching network of the transistor.

2.1.2 OUTPUT MATCHING

Similar steps were undertaken for the output matching network.

The TX tool calculations were as follows:


TXLINE 2003 - Microstrip

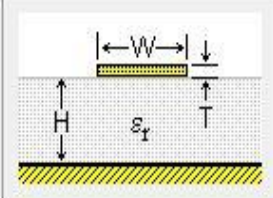
Microstrip | Stripline | CPW | CPW Ground | Round Coaxial | Slotline | Coupled MSLine | Coupled Stripline

Material Parameters

Dielectric: RT/Duroid 5880
 Dielectric Constant: 2.16
 Loss Tangent: 0.001

Conductor: Silver
 Conductivity: 6.14E+07 S/m



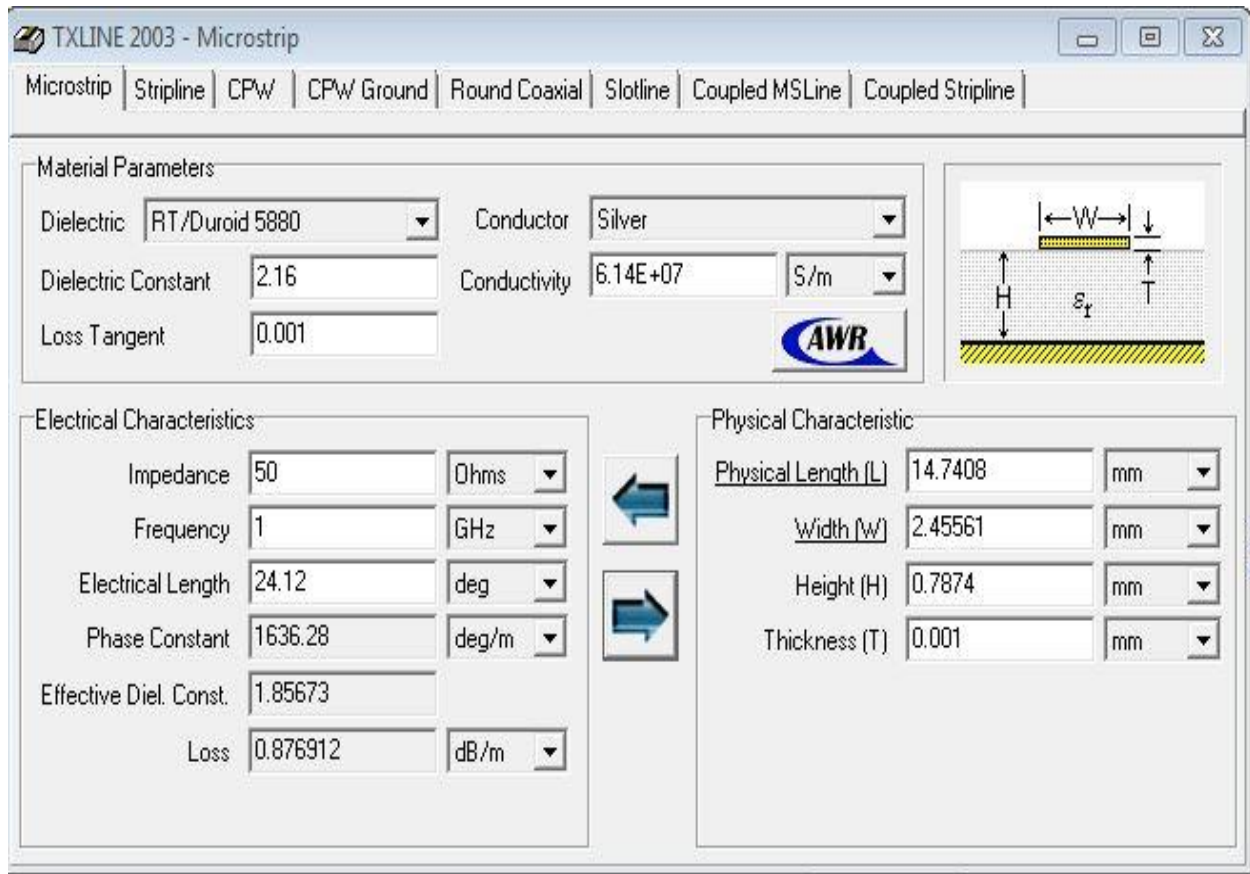


Electrical Characteristics

Impedance: 50 Ohms
 Frequency: 1 GHz
 Electrical Length: 16.92 deg
 Phase Constant: 1636.28 deg/m
 Effective Diel. Const.: 1.85673
 Loss: 0.876912 dB/m

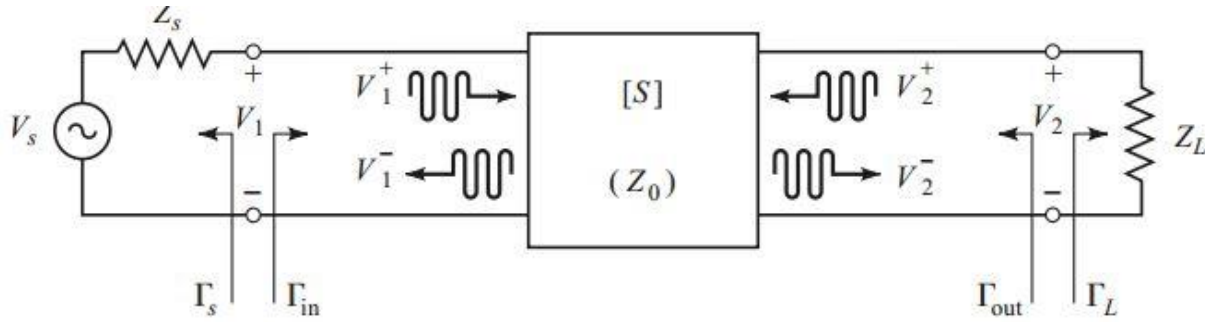
Physical Characteristic

Physical Length (L): 10.3406 mm
 Width (w): 2.45561 mm
 Height (H): 0.7874 mm
 Thickness (T): 0.001 mm



2.1.3 POWER GAINS

There are types of power gains to consider when constructing an amplifier. Consider the below two port network for illustration purposes.



RE 12.1 A two-port network with arbitrary source and load impedances.

Two port power gains:

1. **Power gain** $= G = P_L / P_{in}$ is the ratio of power dissipated in the load Z_L to the power delivered to the input of the two-port network. This gain is independent of Z_S , although the characteristics of some active devices may be dependent on Z_S .

2. **Available power gain** $= G_A = P_{avn} / P_{avs}$ is the ratio of the power available from the two-port network to the power available from the source. This assumes conjugate matching of both the source and the load, and depends on Z_S , but not Z_L .

3. **Transducer power gain** $= G_T = P_L / P_{avs}$ is the ratio of the power delivered to the load to the power available from the source. This depends on both Z_S and Z_L .

ReflectionL=

$$Z_L - Z_0 / Z_L + Z_0 \dots \dots \dots \text{eqn 1.}$$

ReflectionS=

$Z_S - Z_0 / Z_S + Z_0$eqn2.

Average power delivered to the network is:

$$P_{in} = \frac{1}{2Z_0} |V_1^+|^2 (1 - |\Gamma_{in}|^2) = \frac{|V_S|^2}{8Z_0} \frac{|1 - \Gamma_S|^2}{|1 - \Gamma_S \Gamma_{in}|^2} (1 - |\Gamma_{in}|^2),$$

Average power delivered to the load is:

$$P_L = \frac{|V_2^-|^2}{2Z_0} (1 - |\Gamma_L|^2).$$

Whereas **power gain** can be expressed as follows:

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2) |1 - S_{22} \Gamma_L|^2}.$$

The power available from the source, P_{avs} , is the maximum power that can be delivered to the network. This occurs when the input impedance of the terminated network is conjugately matched to the source impedance.

$$P_{avs} = P_{in} \Big|_{\Gamma_{in}=\Gamma_S^*} = \frac{|V_S|^2}{8Z_0} \frac{|1 - \Gamma_S|^2}{(1 - |\Gamma_S|^2)}.$$

Similarly, the power available from the network, P_{avn} , is the maximum power that can be delivered to the load.

$$P_{avn} = \frac{|V_S|^2}{8Z_0} \frac{|S_{21}|^2 |1 - \Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2 (1 - |\Gamma_{out}|^2)}.$$

Observe that P_{avs} and P_{avn} have been expressed in terms of the source voltage, V_S , which is independent of the input or load impedances. There would be confusion if these quantities were expressed in terms of $V+1$, since $V+1$ is different for each of the calculations of P_L , P_{avs} , and P_{avn} .

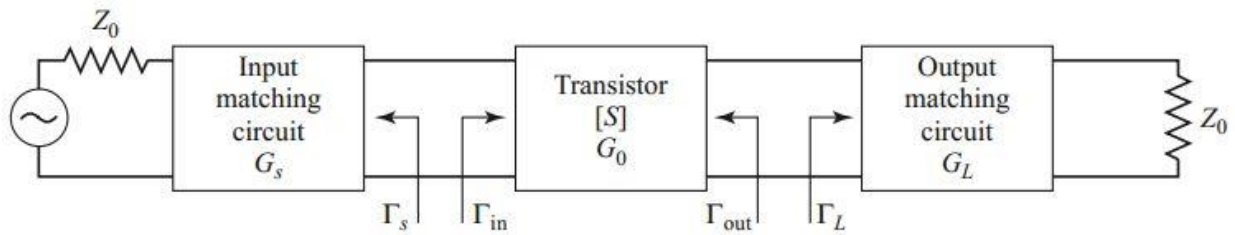
We now obtain the available power gain as

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2 (1 - |\Gamma_{out}|^2)}.$$

The transducer power gain is:

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2) (1 - |\Gamma_L|^2)}{|1 - \Gamma_S\Gamma_{in}|^2 |1 - S_{22}\Gamma_L|^2}.$$

A single-stage microwave transistor amplifier can be modeled by the circuit of Figure 3, where matching networks are used on both sides of the transistor to transform the input and output impedance Z_0 to the source and load impedances Z_S and Z_L . The most useful gain definition for amplifier design is the transducer power gain, which accounts for both source and load mismatch.



Using the above Figure 3, the gains are calculated as follows:

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2},$$

$$G_0 = |S_{21}|^2,$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}.$$

2.1.4 STABILITY.

We now discuss the necessary conditions for a transistor amplifier to be stable. In the circuit of Figure 12.2, oscillation is possible if either the input or output port impedance has a negative real part; this would then imply that $|\text{REFLECTION}_{in}| > 1$ or $|\text{REFLECTION}_{out}| > 1$. Because REF_{in} and REF_{out} depend on the source and load matching networks, the stability of the amplifier depends on REF_S and REF_L as presented by the matching networks. Thus, we define two types of stability:

1. Unconditional stability: The network is unconditionally stable if $|\text{REF}_{in}| < 1$ and

$|\Gamma_{out}| < 1$ for all passive source and load impedances (i.e., $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).

2. Conditional stability: The network is conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

Note that the stability condition of an amplifier circuit is usually frequency dependent since the input and output matching networks generally depend on frequency. It is therefore possible for an amplifier to be stable at its design frequency but unstable at other frequencies. Careful amplifier design should consider this possibility.

Applying the above requirements for unconditional stability gives the following conditions that must be satisfied by Γ_S and Γ_L if the amplifier is to be unconditionally stable:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1,$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1.$$

If the device is unilateral ($S_{12}=0$), these conditions reduce to the simple results that

$|S_{11}| < 1$ and $|S_{22}| < 1$ are sufficient for unconditional stability. Otherwise, the inequalities above define a range of values for REFS and REF L where the amplifier will be stable.

Finding this range for REF S and REF L can be facilitated by using the Smith chart and plotting the input and output stability circles. The stability circles are defined as the loci in the REFL(or S) plane for which $|REF\ in|=1$ (or $|REF\ out|=1$). The stability circles then define the boundaries between stable and potentially unstable regions of REF Sand REFL. REF S and REF L must lie on the Smith chart ($|REF\ S| < 1, |REF\ L| < 1$ for passive matching networks).

Stability circle with a center C_L and radius R_L is easily defined with the expressions:

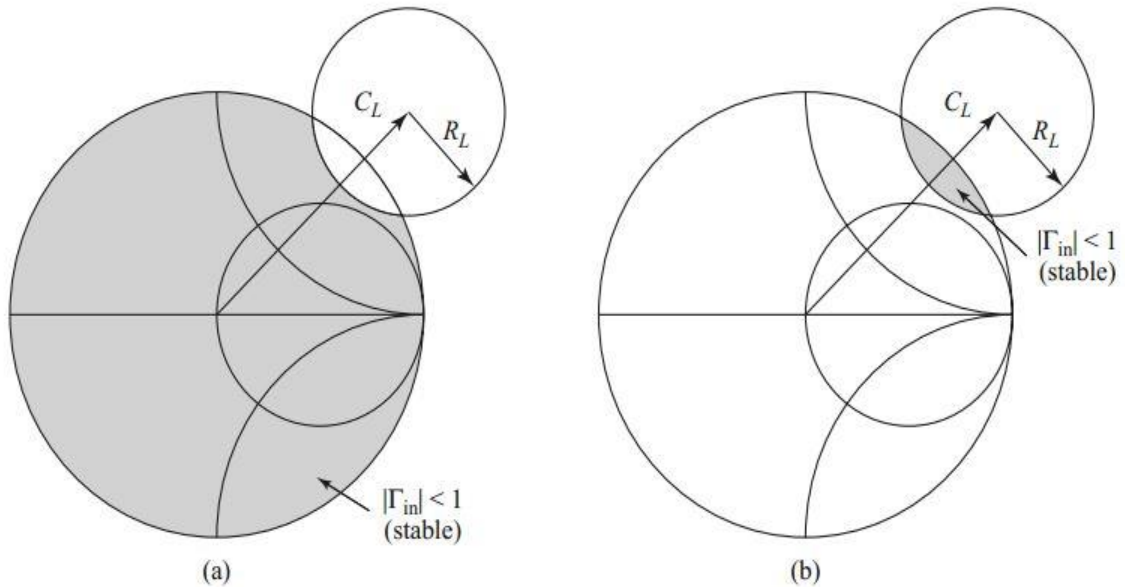
$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad (\text{center}),$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (\text{radius}).$$

If the device is unconditionally stable, the stability circles must be completely outside (Or totally enclose) the Smith chart

$$|C_L - R_L| > 1 \quad \text{for} \quad |S_{11}| < 1, \quad (12.27a)$$

$$|C_S - R_S| > 1 \quad \text{for} \quad |S_{22}| < 1. \quad (12.27b)$$



Stability circles demonstrating stability.

The stability circles discussed above can be used to determine regions for REF S and REF L where the amplifier circuit will be conditionally stable, but simpler tests can be used to determine unconditional stability. It can be shown that a device will be unconditionally stable if Rollet's condition, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1,$$

Where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1,$$

This condition if satisfied gives an unconditionally stable amplifier.

2.1.5 NOISE CONSIDERATIONS.

Besides stability and gain, another important design consideration for a microwave amplifier is its noise figure. In receiver applications especially it is often required to have a preamplifier with as low a noise figure as possible, the first stage of a receiver front end has the dominant effect on the noise performance of the over-all system. Generally it is not possible to obtain both minimum noise figure and maximum

gain for an amplifier, so some sort of compromise must be made. This can be done by using constant-gain circles and circles of constant noise figure to select a usable trade-off between noise figure and gain. Here we will derive the equations for constant-noise figure circles and show how they are used in transistor amplifier design.

The noise figure of a two-port amplifier can be expressed as

$$F = F_{\min} + \frac{R_N}{G_S} |Y_S - Y_{\text{opt}}|^2, \quad (1.3)$$

where the following definitions apply:

$Y_S = G_S + jB_S$ = source admittance presented to transistor.

Y_{opt} = optimum source admittance that results in minimum noise figure.

F_{\min} = minimum noise figure of transistor, attained when $Y_S = Y_{\text{opt}}$.

R_N = equivalent noise resistance of transistor.

G_S = real part of source admittance.

Instead of the admittance Y_S and Y_{opt} , we can use the reflection coefficients Γ_S and Γ_{opt} ,

Where

$$Y_S = \frac{1}{Z_0} \frac{1 - \Gamma_S}{1 + \Gamma_S},$$
$$Y_{opt} = \frac{1}{Z_0} \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}}.$$

Γ_S is the source reflection coefficient. The quantities F_{min} , Γ_{opt} and R_N are characteristics of the particular transistor being used, and are called the noise

Parameters of the device; they may be given by the manufacturer or measured.

Using the above equation, we can express the quantity $|Y_S - Y_{opt}|^2$

in terms of Γ_S and Γ_{opt} :

$$|Y_S - Y_{opt}|^2 = \frac{4}{Z_0^2} \frac{|\Gamma_S - \Gamma_{opt}|^2}{|1 + \Gamma_S|^2 |1 + \Gamma_{opt}|^2}.$$

In addition

$$G_S = \text{Re}\{Y_S\} = \frac{1}{2Z_0} \left(\frac{1 - \Gamma_S}{1 + \Gamma_S} + \frac{1 - \Gamma_S^*}{1 + \Gamma_S^*} \right) = \frac{1}{Z_0} \frac{1 - |\Gamma_S|^2}{|1 + \Gamma_S|^2}.$$

Using these results in equation 12.3, Gives the noise figure as

$$F = F_{\min} + \frac{4R_N}{Z_0} \frac{|\Gamma_S - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_S|^2)|1 + \Gamma_{\text{opt}}|^2}. \quad (1.3a)$$

For a fixed noise figure F we can show that this result defines a circle in the REFS plane.

First define the noise figure parameter, N, as

$$N = \frac{|\Gamma_S - \Gamma_{\text{opt}}|^2}{1 - |\Gamma_S|^2} = \frac{F - F_{\min}}{4R_N/Z_0} |1 + \Gamma_{\text{opt}}|^2, \quad (1.3b)$$

which is a constant for a given noise figure and set of noise parameters. Then rewrite

(1.3b)

$$\begin{aligned}
 (\Gamma_S - \Gamma_{\text{opt}})(\Gamma_S^* - \Gamma_{\text{opt}}^*) &= N(1 - |\Gamma_S|^2), \\
 \Gamma_S \Gamma_S^* - (\Gamma_S \Gamma_{\text{opt}}^* + \Gamma_S^* \Gamma_{\text{opt}}) + \Gamma_{\text{opt}} \Gamma_{\text{opt}}^* &= N - N|\Gamma_S|^2, \\
 \Gamma_S \Gamma_S^* - \frac{(\Gamma_S \Gamma_{\text{opt}}^* + \Gamma_S^* \Gamma_{\text{opt}})}{N + 1} &= \frac{N - |\Gamma_{\text{opt}}|^2}{N + 1}.
 \end{aligned}$$

Add $|\Gamma_{\text{opt}}|^2/(N+1)^2$ to both sides to complete the square to obtain

$$\left| \Gamma_S - \frac{\Gamma_{\text{opt}}}{N + 1} \right| = \frac{\sqrt{N(N + 1 - |\Gamma_{\text{opt}}|^2)}}{(N + 1)}.$$

This result defines circles of constant noise figure with centers at

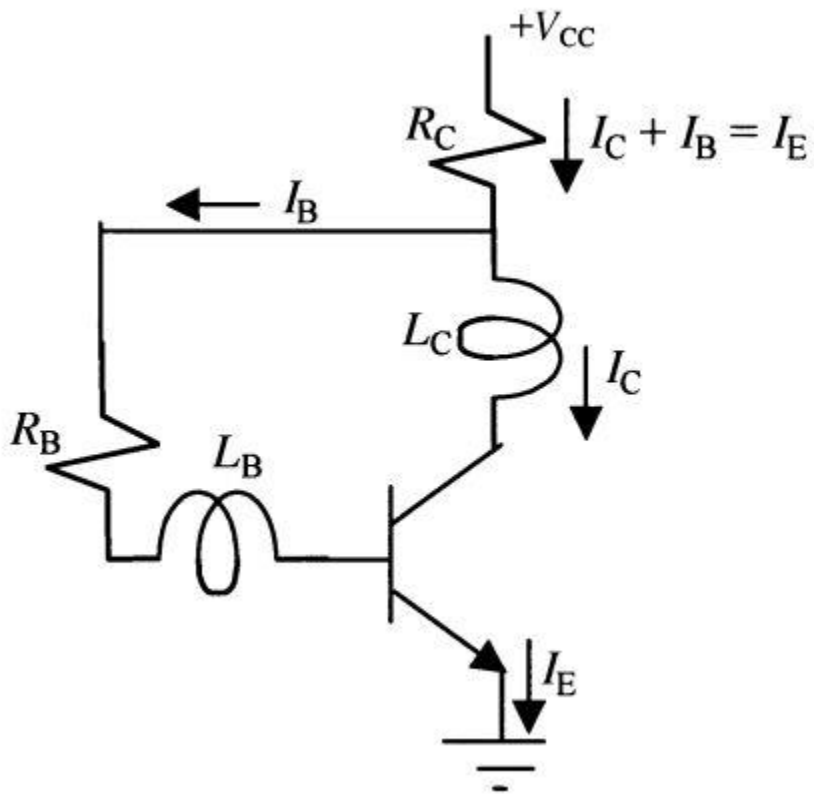
$$C_F = \frac{\Gamma_{\text{opt}}}{N + 1},$$

and radii of

$$R_F = \frac{\sqrt{N(N + 1 - |\Gamma_{\text{opt}}|^2)}}{N + 1}.$$

2.1.6 DC BIAS CIRCUITS FOR TRANSISTORS

Transistor circuits require dc bias that provides the desired quiescent point. Further, it should hold the operation stable over a range of temperatures. Resistive circuits used at lower frequencies can be employed in the RF range as well. However, sometimes these circuits may not work satisfactorily at higher frequencies. For example, a resistance in parallel with a bypass capacitor is frequently used at the emitter to provide stable operation at lower frequencies. This circuit may not work at microwave frequencies because it can produce oscillations. Active bias networks provide certain advantages over resistive circuits.



The figure above illustrates a resistive bias network with voltage feedback. Inductors L_C and L_B are used to block RF from going toward R_C and R_B . At the same time, dc bias passes through them to respective terminals of BJT without loss. If V_{be} represent base-emitter voltage of the transistor then

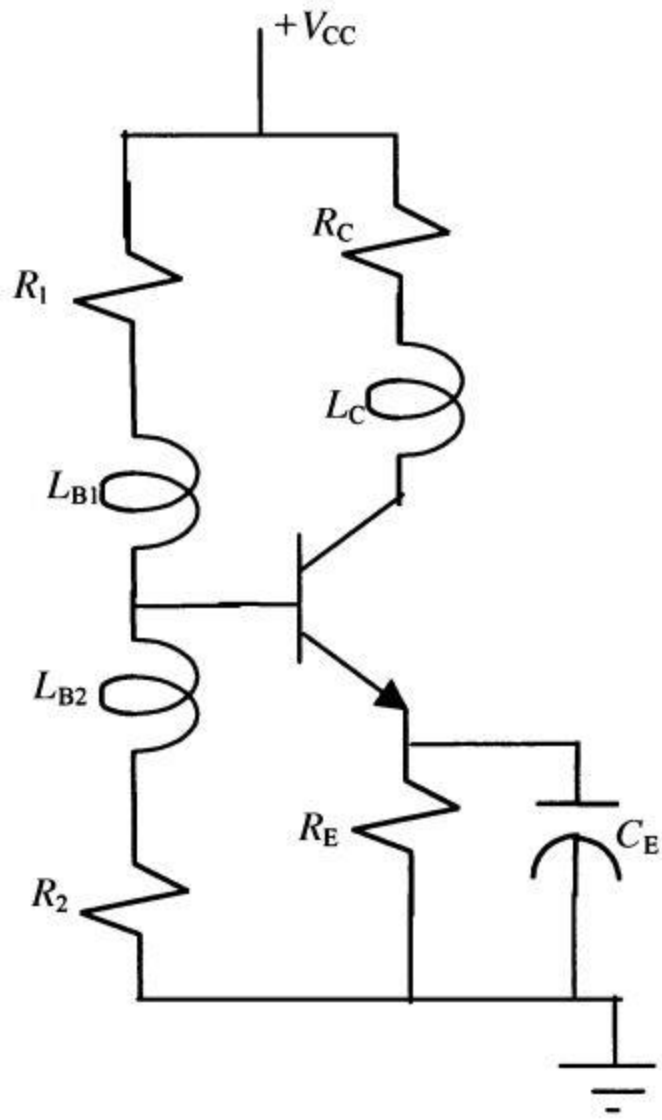
$$V_{BE} + R_B I_B + R_C I_E = V_{CC}$$

Since

$$I_B = I_E - I_C = (1 - \alpha)I_E = \frac{I_E}{1 + \beta}$$

This can be rewritten as follows:

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{1 + \beta}}$$



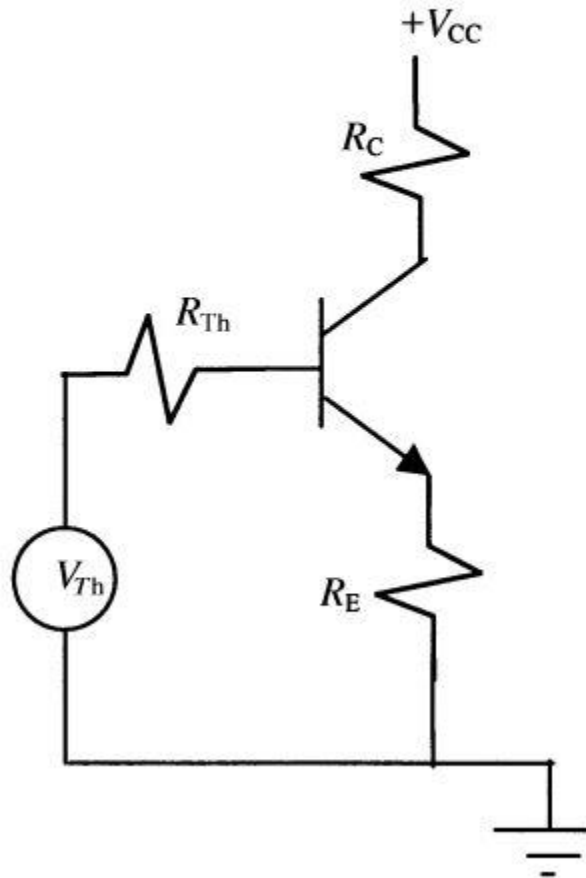
Transistor bias circuit with emitter bypassed resistor. fig 1.3d

For I_E to be less sensitive to changes in V_{BE} and β , the following conditions must be satisfied:

$$V_{CC} \gg V_{BE}$$

And

$$R_C \gg \frac{R_B}{1 + \beta}$$



Hence , it is advisable to use high V_{cc} and R_c . However, there are practical limitations. Another option is to use a small R_b , but it will limit V_{ce} and, therefore, the swing in output. It is up to the circuit designer to weigh these options of the trade-off and pick the components accordingly.

An alternative biasing network that uses a bypassed resistor at the emitter is illustrated in fig 1.3b. As before, inductors L_c , L_{b1} and L_{b2} are used to block the RF. On the other hand, capacitor C_e is used to bypass RF. The next figure shows the equivalent thevenin circuit for dc condition where

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and,

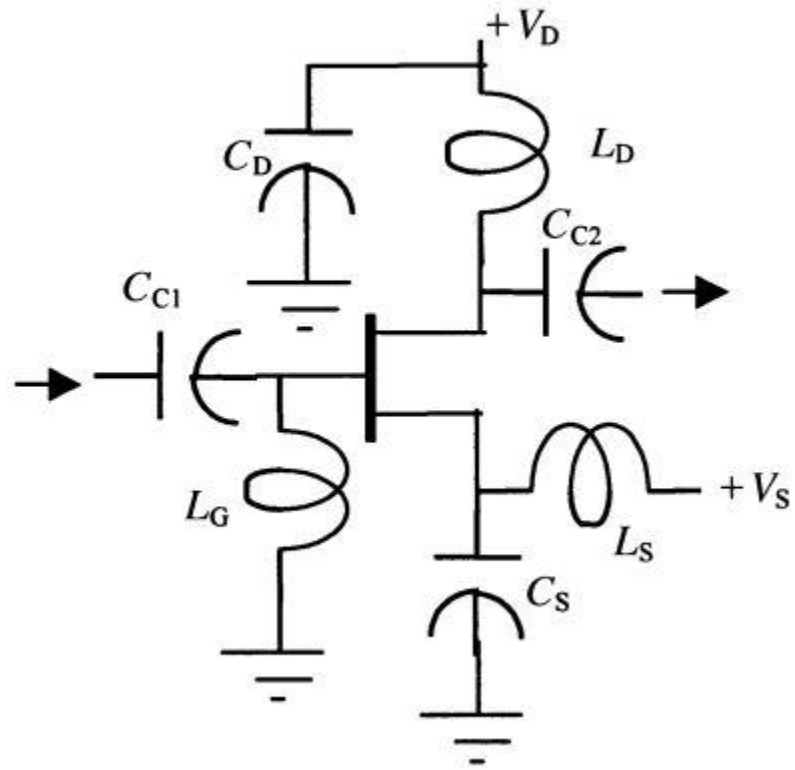
$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

From the equivalent circuit shown:

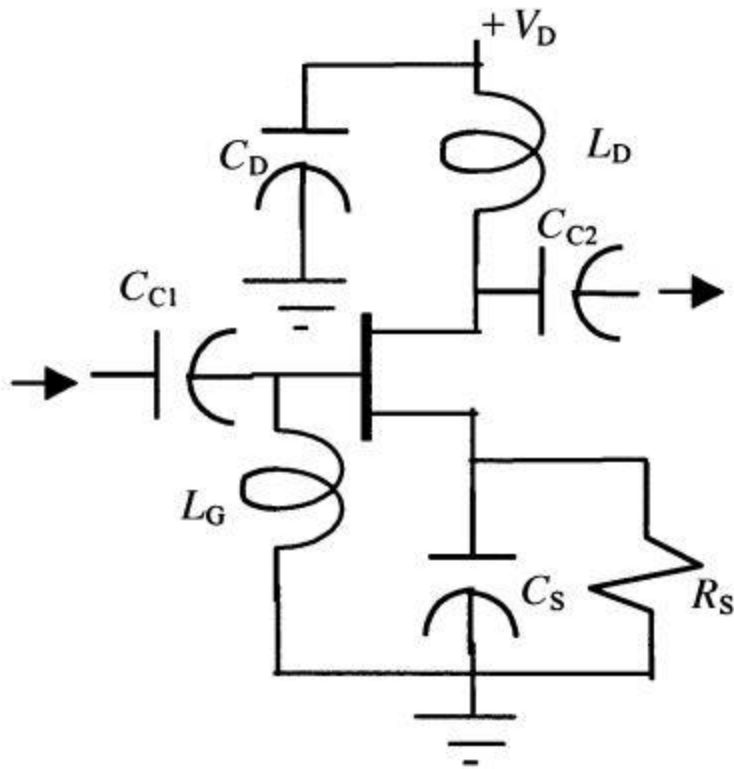
$$V_{Th} = R_{Th} I_B + V_{BE} + R_E I_E = \left(\frac{R_{Th}}{1 + \beta} + R_E \right) I_E + V_{BE}$$

Hence,

$$I_E = \frac{V_{Th} - V_{BE}}{R_E + \frac{R_{Th}}{1 + \beta}}$$



A bias circuit employing two unipolar dc sources .



Transistor bias circuit employing a single power supply.

Therefore, the following conditions must be met for stable I_e :

$$V_{Th} \gg V_{BE}$$

and,

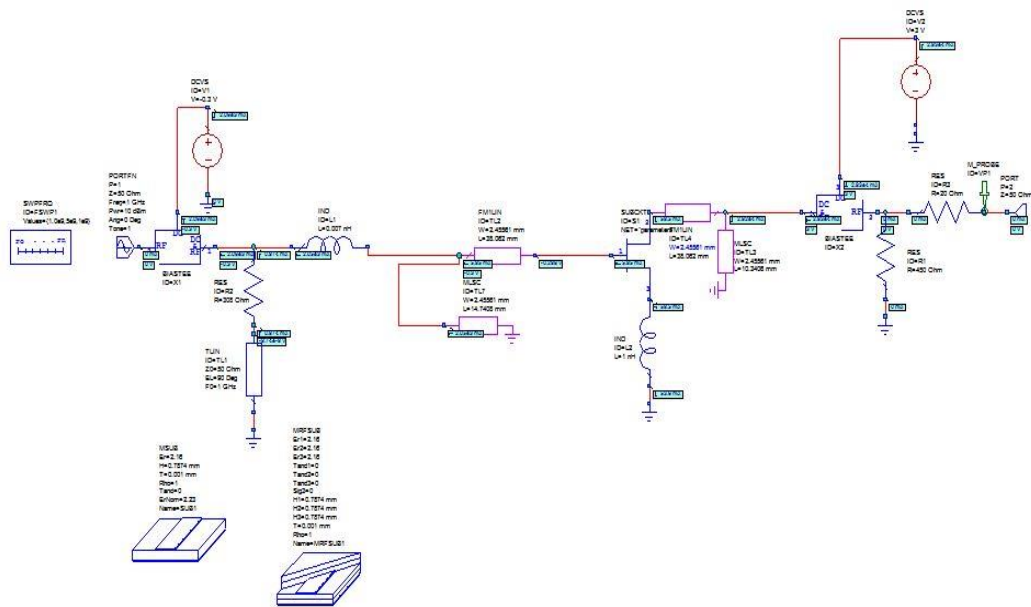
$$R_E \gg \frac{R_{Th}}{1 + \beta}$$

Note that for a fixed V_{cc} , V_{th} cannot be increased arbitrarily because it reduces V_{cb} and hence V_{ce} . Smaller V_{ce} means limited output swing. Further, Large R_e will reduce V_{ce} as well. On the other hand, smaller R_{th} will mean low input impedance of the circuit. As a rule of thumb, V_{th} is selected no more than 15 to 20 percent of V_{cc}

CHAPTER 3: DESIGN

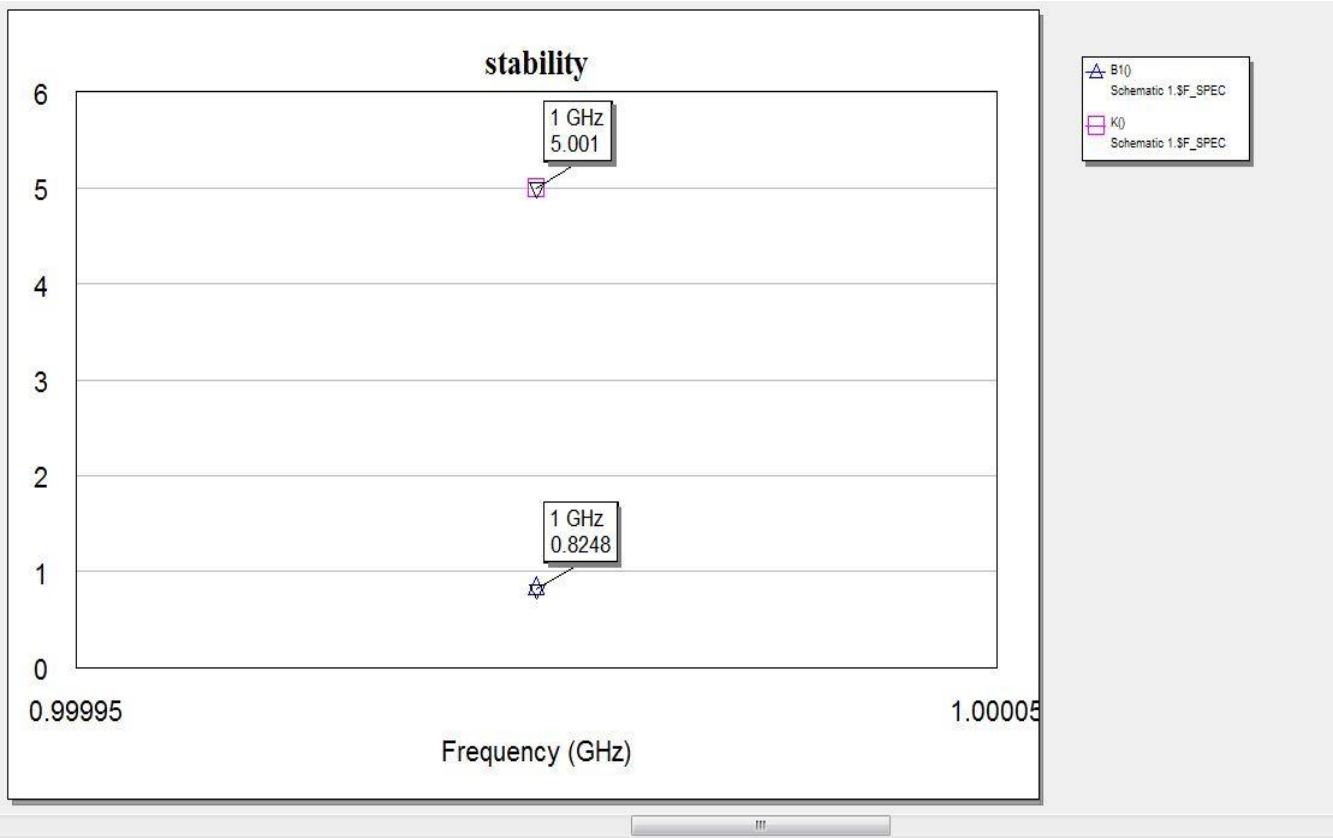
3.1 LOW NOISE AMPLIFIER DESIGN

Simulation diagrams used to achieve low noise amplifier:



AWR schematic used to achieve the amplification of 1Ghz frequency.

Stability graph showing the schematic is stable at the frequency is shown below:

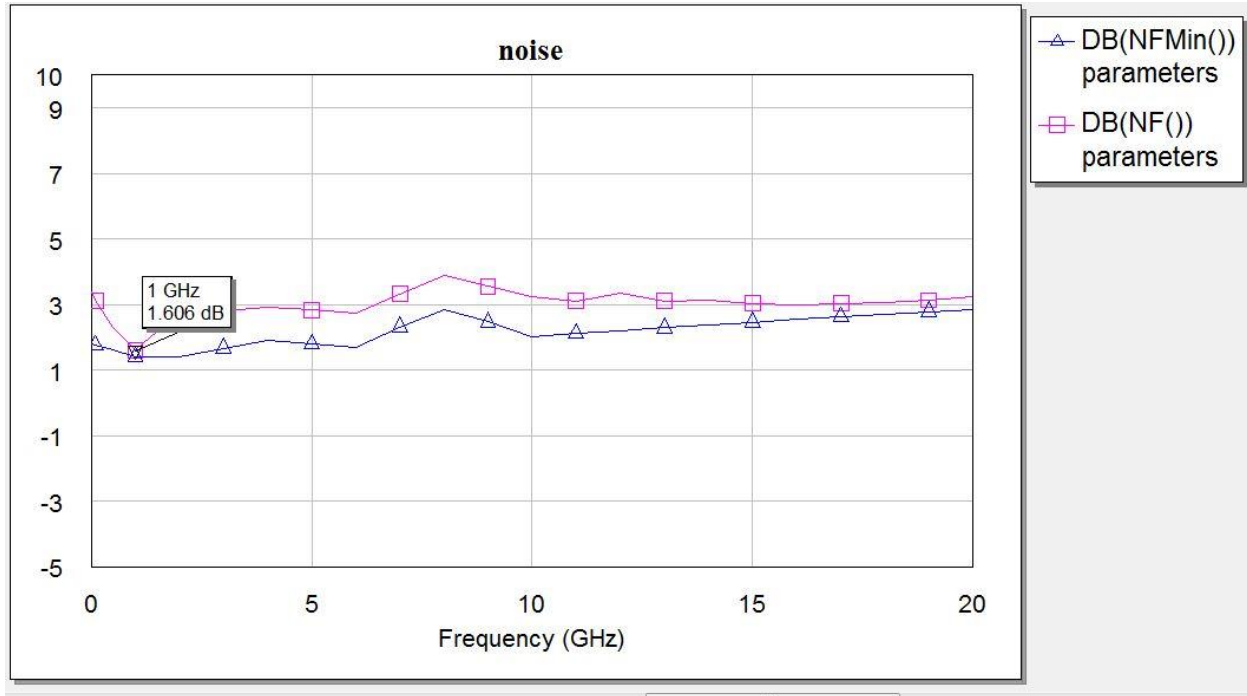


Using the auto graph configuration for the particular frequency, the value for K is seen to be above 1 as required by the Rollet 's condition for the system to be stable.

This is show by the marker as 5.001 at the frequency of operation.

3.1.1 NOISE OF THE SCHEMATIC .

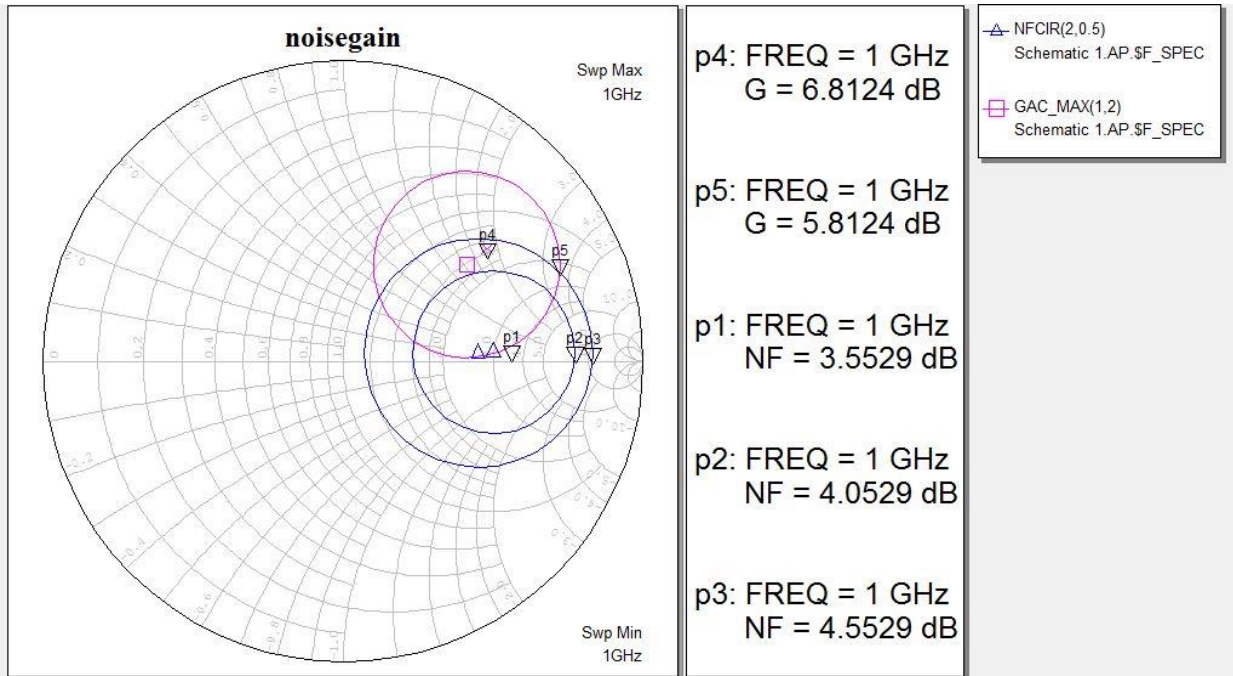
The noise graph curve is shown below:



The noise is at its lowest in the operating frequency which is 1Ghz.The recorded value is 1.606dB which means that very minimal noise is picked within the circuit.

3.1.2 NOISE FIGURE

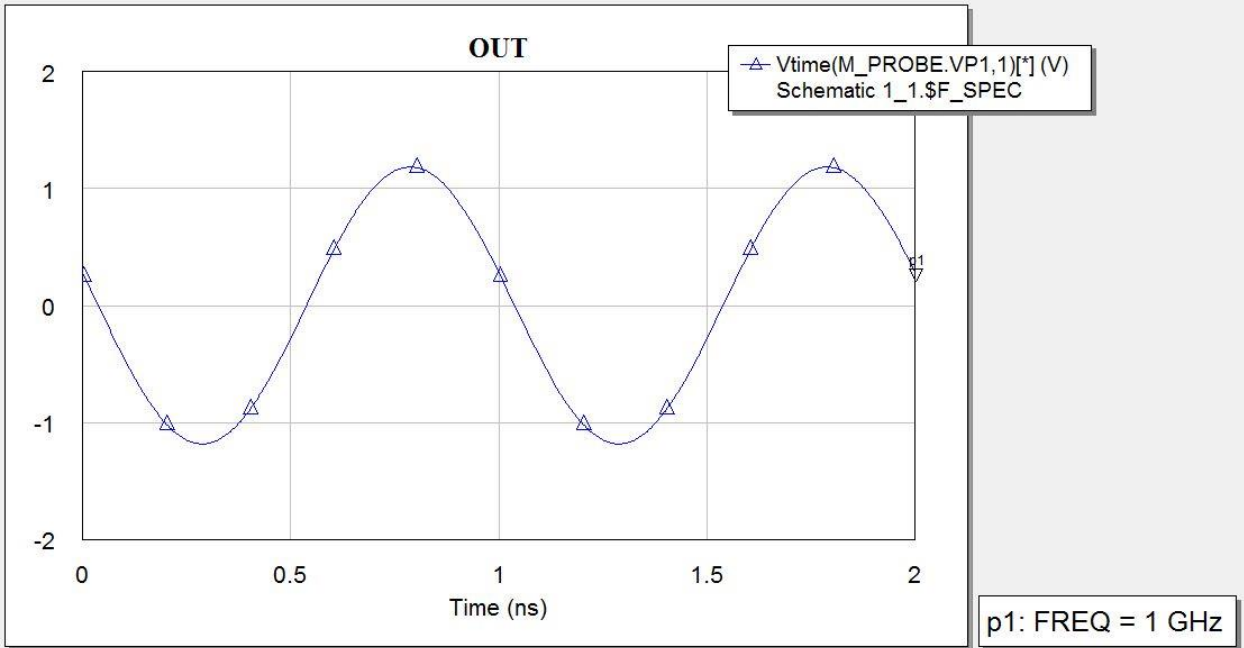
The noise figure graph is shown below :



The above from AWR shows the schematic noise figure-gain trade-off graph which the schematic relies on to produce optimum gain and minimum noise.

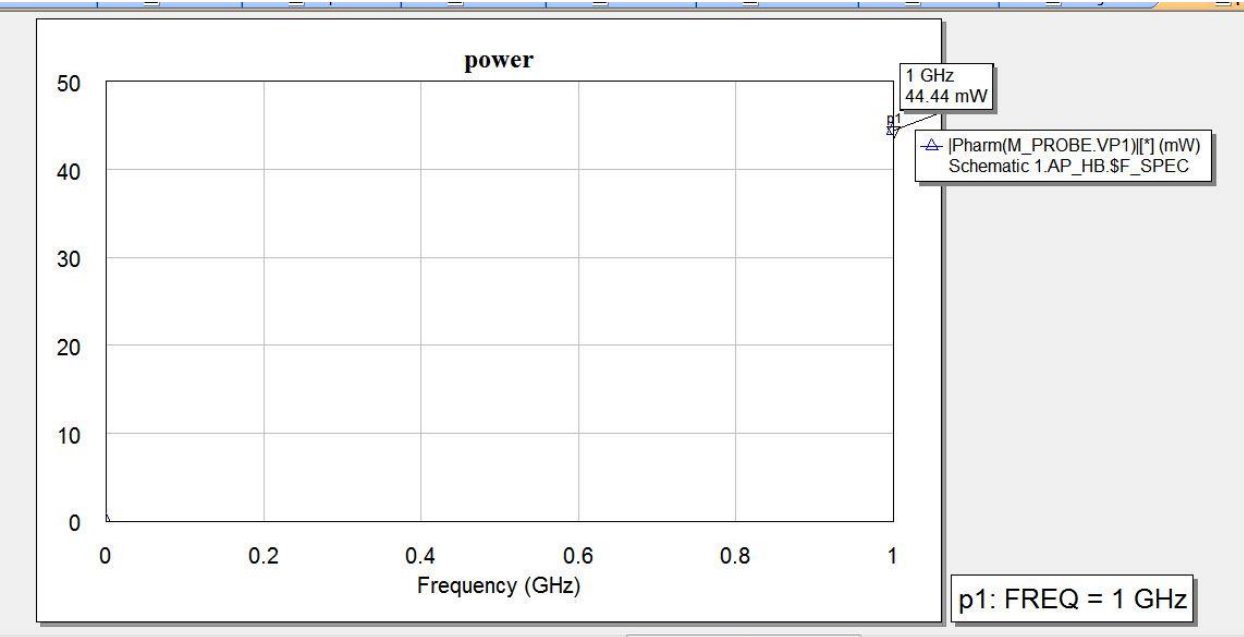
3.1.3 OUTPUT

The output of the schematic was traced by the AWR environment as follows:



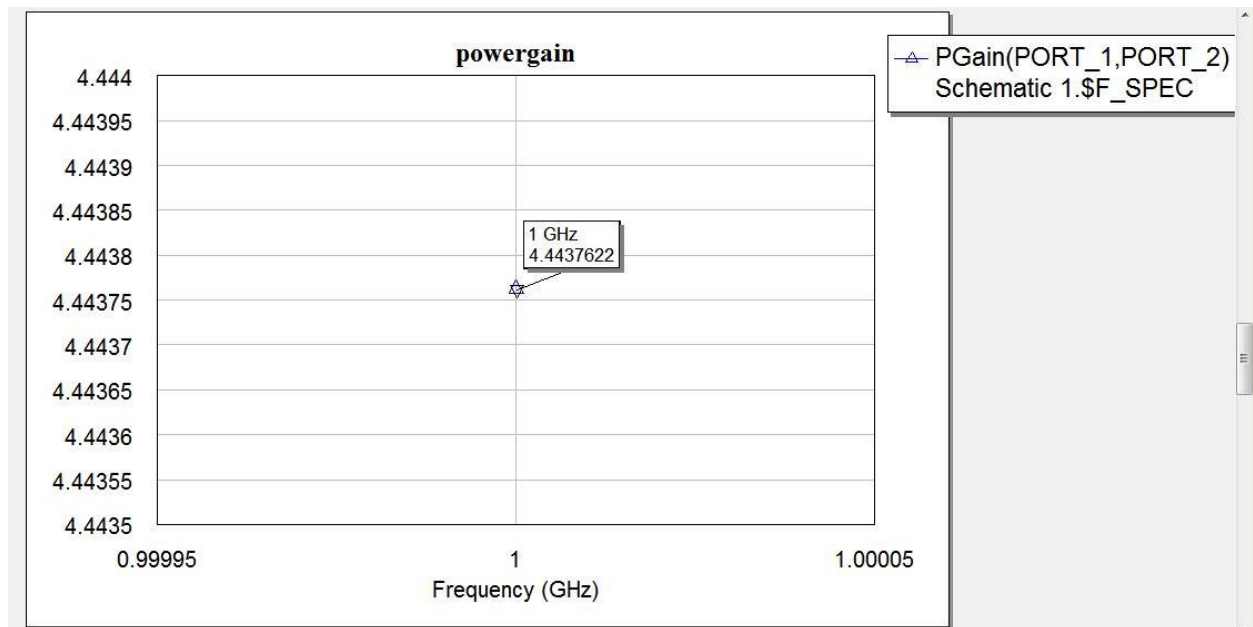
POWER HARMONICS:

The power harmonics graph is as shown below:



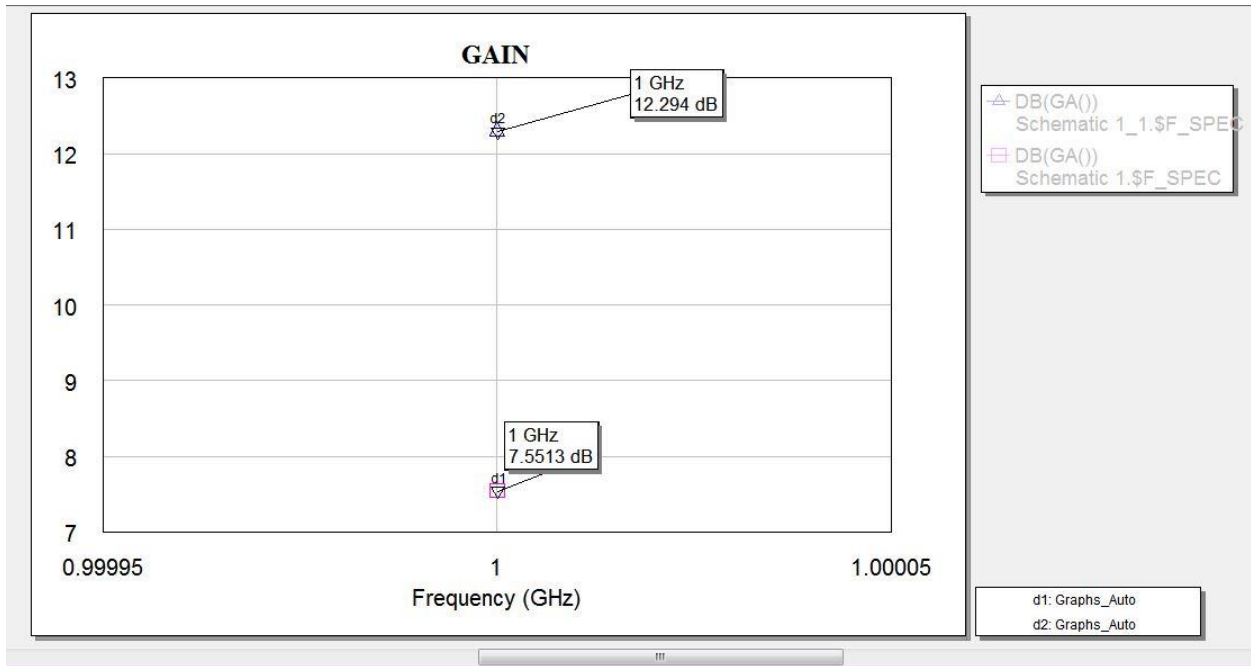
Power harmonics.

This gives the power gain graph below:



Power gain graph of the amplifier.

Gain of the amplifier was 12.7 dB as shown in the graph below. This is expected as it is a single stage amplifier. For a single stage amplifier a gain of minimum 10dB is sufficient.



Amplifier gain graph.

3.2 OSCILLATOR DESIGN AND ANALYSIS

Oscillators are a class of circuits with 1 terminal or port, which produce a periodic electrical output upon power up.

- Most of us would have encountered oscillator circuits while studying for our basic electronics classes.

- Oscillators can be classified into two types:

(A) Relaxation oscillators

and

(B) Harmonic oscillators.

- Relaxation oscillators (also called astable multivibrator), is a class of

circuits with two unstable states. The circuit switches back-and-forth between these states. The output is generally square waves.

- Harmonic oscillators are capable of producing near sinusoidal output, and is based on positive feedback approach.
- Here we will focus on Harmonic Oscillators for RF systems.

Harmonic oscillators are used as this class of circuits are capable of producing stable sinusoidal waveform with low phase noise.

We can view an oscillator as an amplifier that produces an output when there is no input.

- Thus it is an unstable amplifier that becomes an oscillator!
- For example let's consider a conditionally stable amplifier.
- Here instead of choosing load or source impedance in the stable regions of the Smith Chart, we purposely choose the load or source impedance in the unstable impedance regions. This will result in either $|\Gamma_1| > 1$ or $|\Gamma_2| > 1$.
- The resulting amplifier circuit will be called the Destabilized Amplifier.
- having a reflection coefficient magnitude for Γ_1 or Γ_2

greater than one implies the corresponding port resistance R_1 or R_2 is negative, hence the name for this type of oscillator.

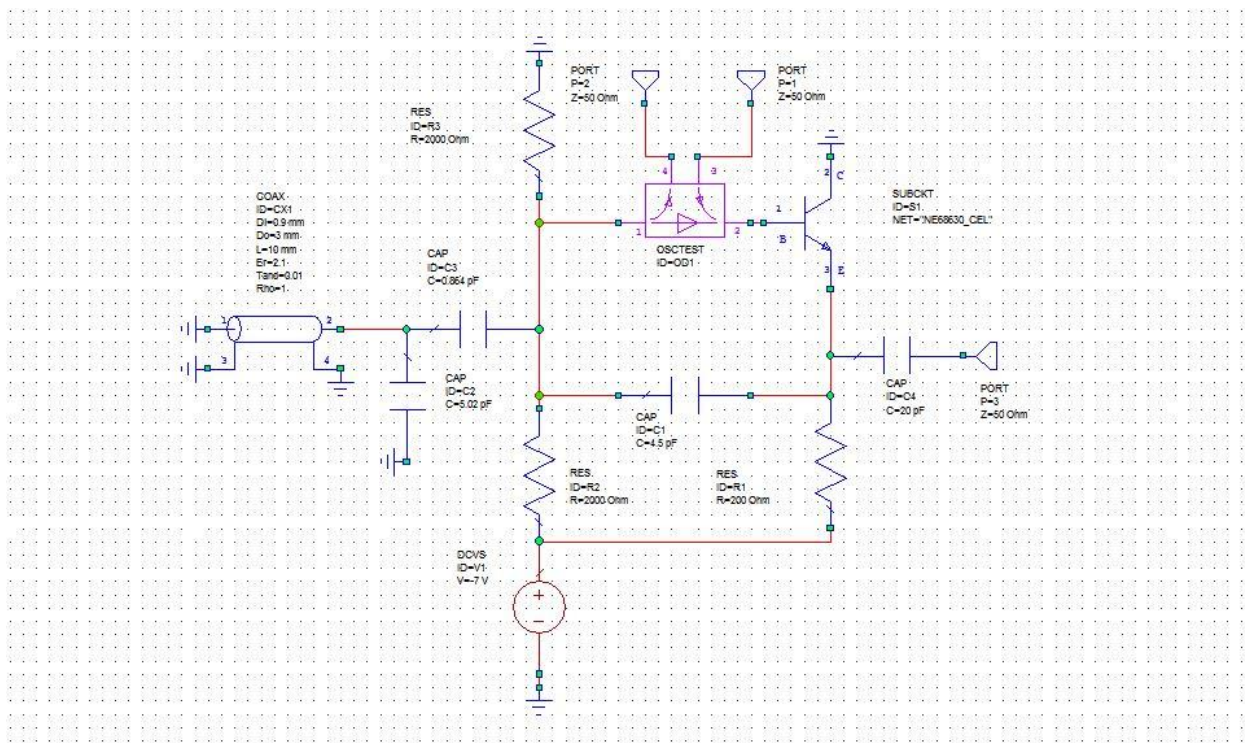
For instance by choosing the load impedance Z_L at the unstable region, we could ensure that $|\Gamma_1| > 1$. We then choose the source impedance

properly so that $|\Gamma_1\Gamma_s| > 1$ and oscillation will start up

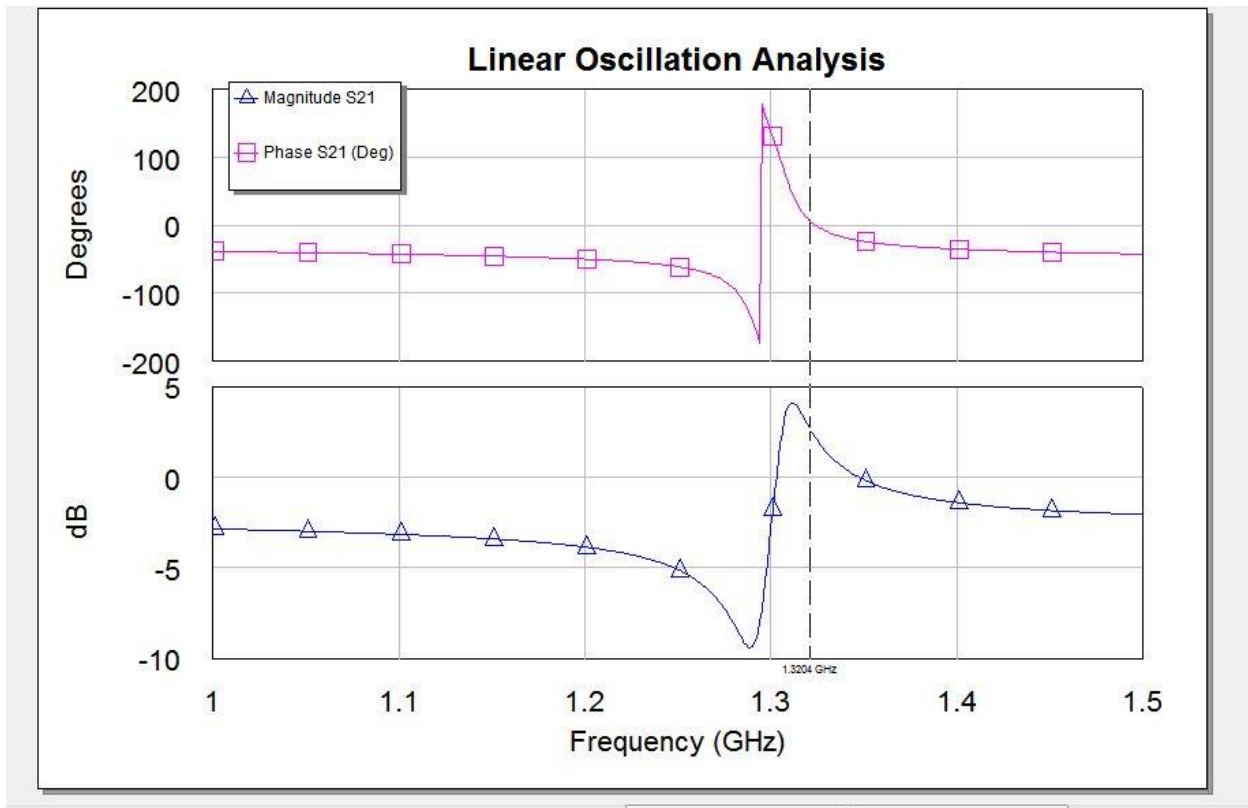
- Once oscillation starts, an oscillating voltage will appear at both the input and output ports of a 2-port network. So it does not matter whether we enforce $|\Gamma_1\Gamma_s| > 1$ or $|\Gamma_2\Gamma_L| > 1$, enforcing either one will cause oscillation to occur (It can be shown later that when $|\Gamma_1\Gamma_s| > 1$ at the input port, $|\Gamma_2\Gamma_L| > 1$ at the output port and vice versa).
- The key to fixed frequency oscillator design is ensuring that the criteria $|\Gamma_1\Gamma_s| > 1$ only happens at one frequency (or a range of intended frequencies), so that no simultaneous oscillations occur at other frequencies.

3.2.1 Step 1 Linear Oscillator schematic

This schematic has the full design with the OSCTEST2 element in the feedback loop to look at the loop characteristics of this circuit. Notice that the direction of the OSCTEST element is into the transistor, which is the forward gain direction. For approximate oscillation conditions to be achieved, the angle of S21 using the OSCTEST will cross the zero angle point when the magnitude of S21 is at a maximum. The phase and magnitude of S21 are shown in the graph “Linear Oscillation Analysis”. This design is very sensitive to the capacitor C1. The original design value is 4.5 pF. Notice with the marker that the approximate oscillation frequency with this circuit is 1.02 GHz.



Oscillator diagram

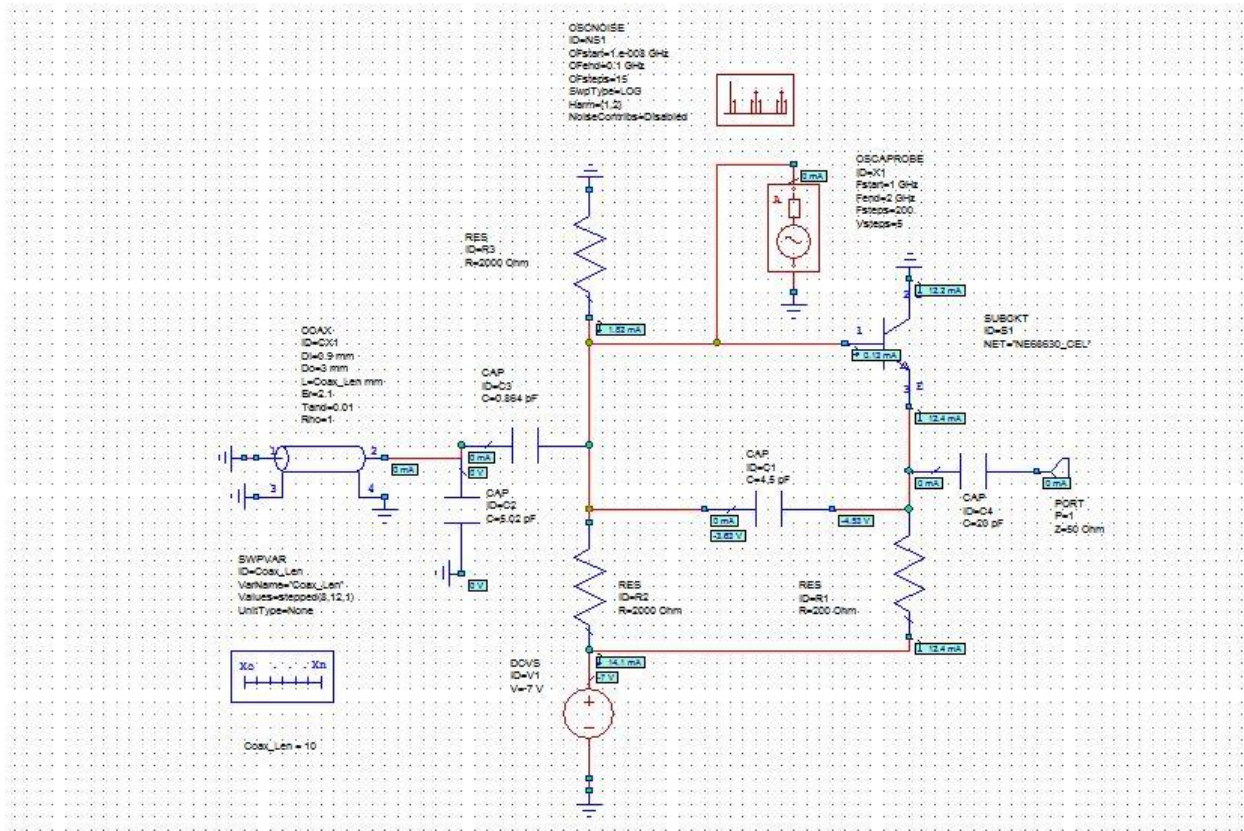


3.2.2 Nonlinear Oscillator schematic

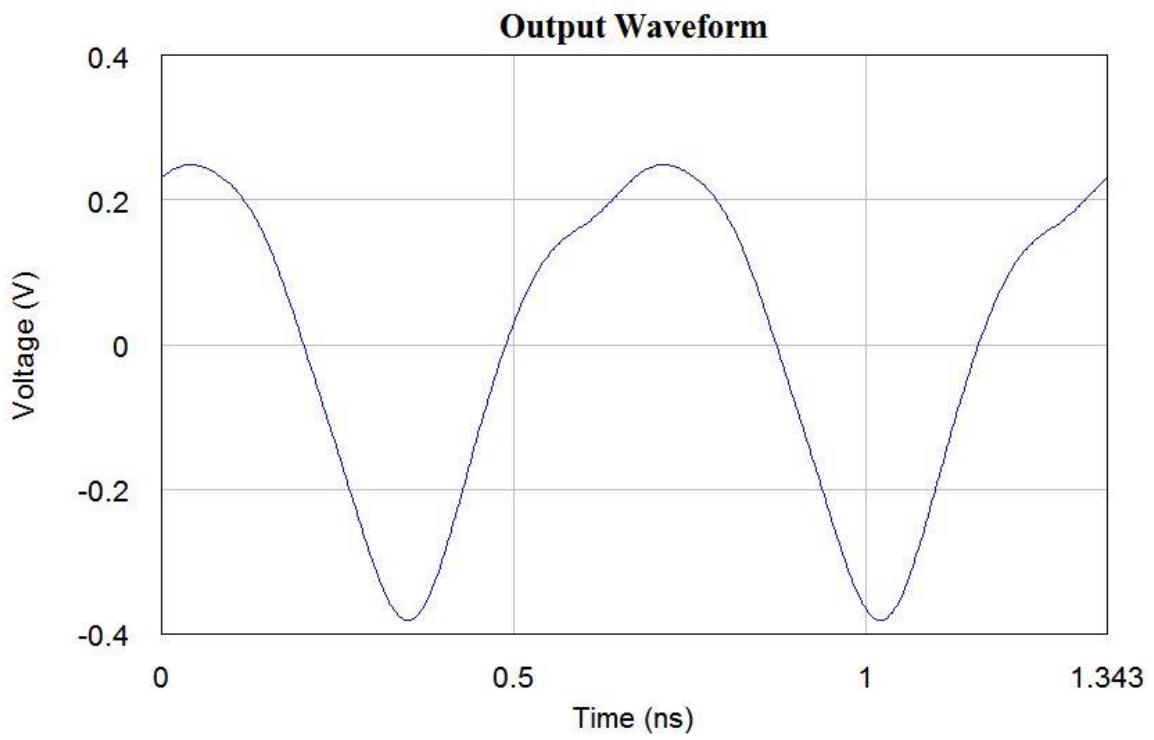
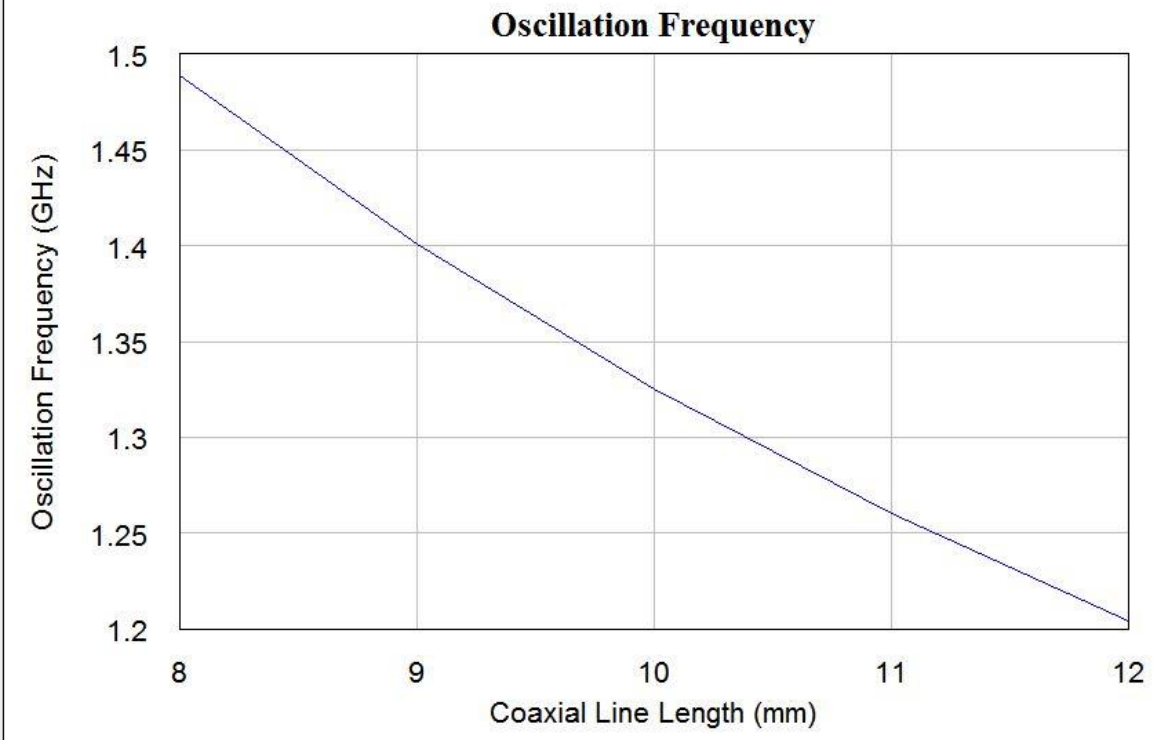
Now that the linear analysis shows that this circuit should oscillate at 1.02 GHz, non-linear oscillator characteristics can be simulated. The OSCTEST element is removed and the OSCAPROBE is hooked into the feedback loop. With this element, the simulator can determine the large signal oscillation frequency, output power and phase noise. Information from the linear analysis is used for setting up the OSCAPROBE element.

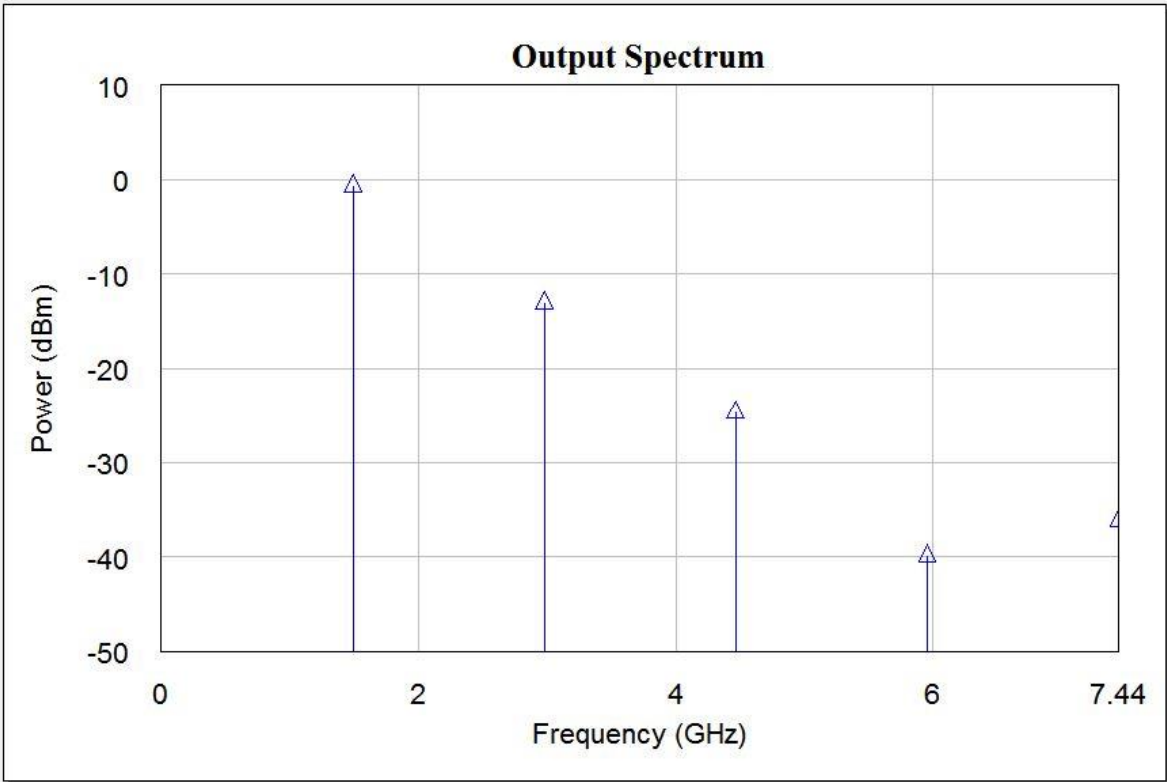
In this design, the coax line in the resonator can be used to set the frequency of oscillation. To help determine the appropriate length of the line to get the right oscillation frequency, the length of this line has been setup as a swept variable to sweep from 8 to 12 mm. The graph "Oscillation Frequency" shows a plot of the oscillation frequency versus the coax line length. You can see that a fairly linear change in oscillation frequency can be achieved by changing this length. Additionally,

notice that when the length is 10 mm (same length as the linear schematic); the oscillation frequency is approximately 1.021 GHz, very close to the linear approximation.



Oscillator diagram



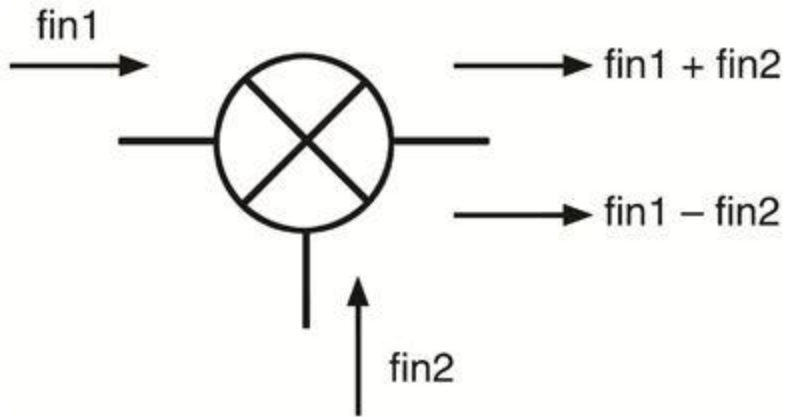


3.3 MIXER

3.3.1 INTRODUCTION

Mixers are used in a variety of RF/microwave applications, including military radar, cellular base stations, and more. An RF mixer is a three-port passive or active device that can modulate or demodulate a signal. The purpose is to change the frequency of an electromagnetic signal while (hopefully) preserving every other characteristic (such as phase and amplitude) of the initial signal. A principal reason for frequency conversion is to allow amplification of the received signal at a frequency other than that of the RF

The three ports are referred to as the RF input port, LO (local oscillator) input port, and the IF (intermediate frequency) output port. A mixer is also known as a down converter if the mixer is part of a receiver or as an up converter if it is part of a transmitter.



Mixer diagram.

Depending upon the application in which the mixer is being used, the LO is typically driven with either a sinusoidal continuous wave signal or a square wave. In concept, the LO signal acts as a gate of the mixer in which the mixer is considered ON when the LO is a large voltage and OFF when it is a small voltage. The LO can only be an input port, while the RF and IF ports can be interchanged between the second input or output.

When the desired frequency is less than the second input frequency, the process is called down conversion. The RF is then the input while the IF is the output. When the desired output frequency is greater than the second input frequency the process is called up conversion. Here the IF is the input while the RF is the output.

In a receiver, when the LO frequency is less than the RF frequency, it is called low-side injection and the mixer is a low-side down converter. When the LO frequency

is above the RF, it is called high-side injection, and the mixer is a high-side down converter.

$$f_{out} = f_{in1} \pm f_{in2}$$

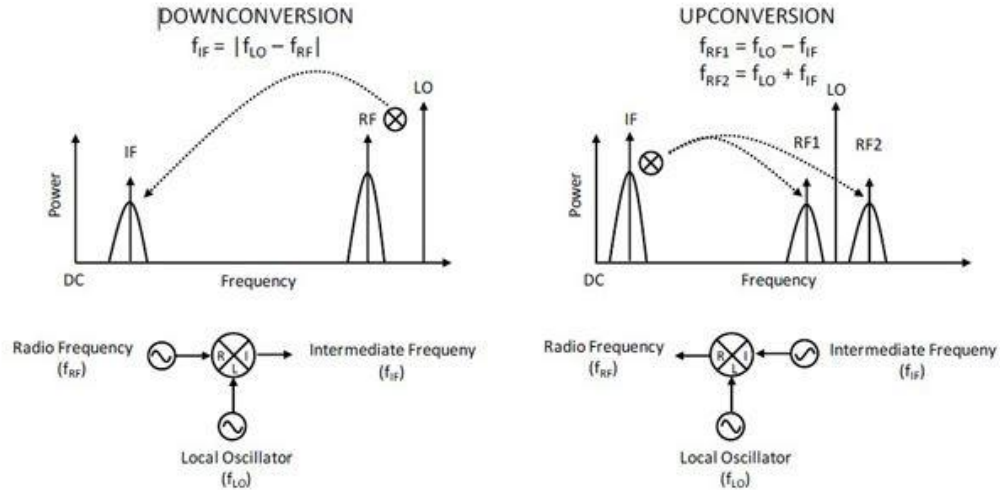


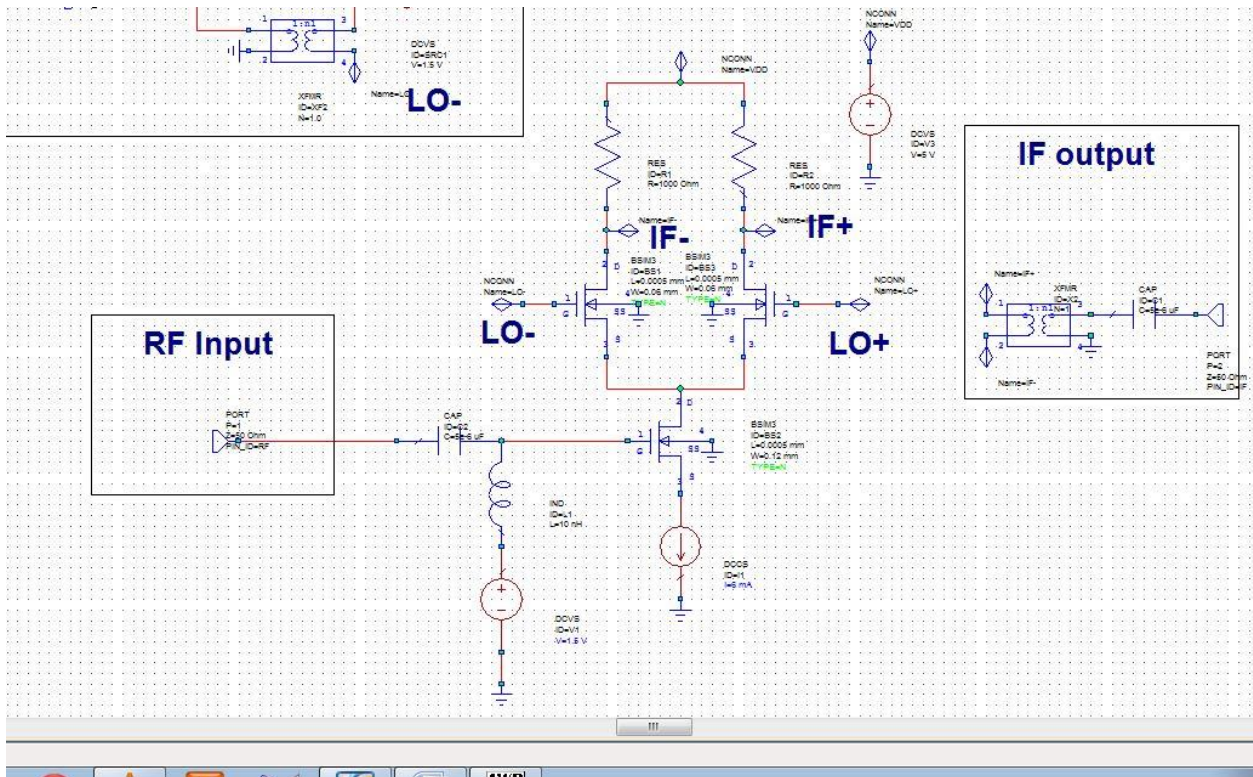
Figure 2: Representation of downconversion and upconversion.

Generally, a passive mixer is made of passive devices, such as diodes. An active mixer is made of active devices, such as transistors. Active or passive implementations are used depending on the application, and there are advantages and disadvantages. As an example, a passive implementation that uses diodes as nonlinear elements or FETs as passive switches, exhibits a conversion loss rather than gain. This may impact the overall noise performance of the system, so in this case an LNA is usually added prior to the mixer.

Passive mixers are widely used due to their simplicity, wide bandwidth, and good inter modulation distortion (IMD) performance. Active mixers are mostly used for RFIC implementation. They are configured to provide conversion gain, good isolation between the signal ports, and require less power to drive the LO port. They can be monolithically integrated with other signal processing circuitry and are less sensitive to load-matching.

3.3.2 DESIGN OF THE MIXER

The mixer circuit from the AWR environment used in the project is shown below:



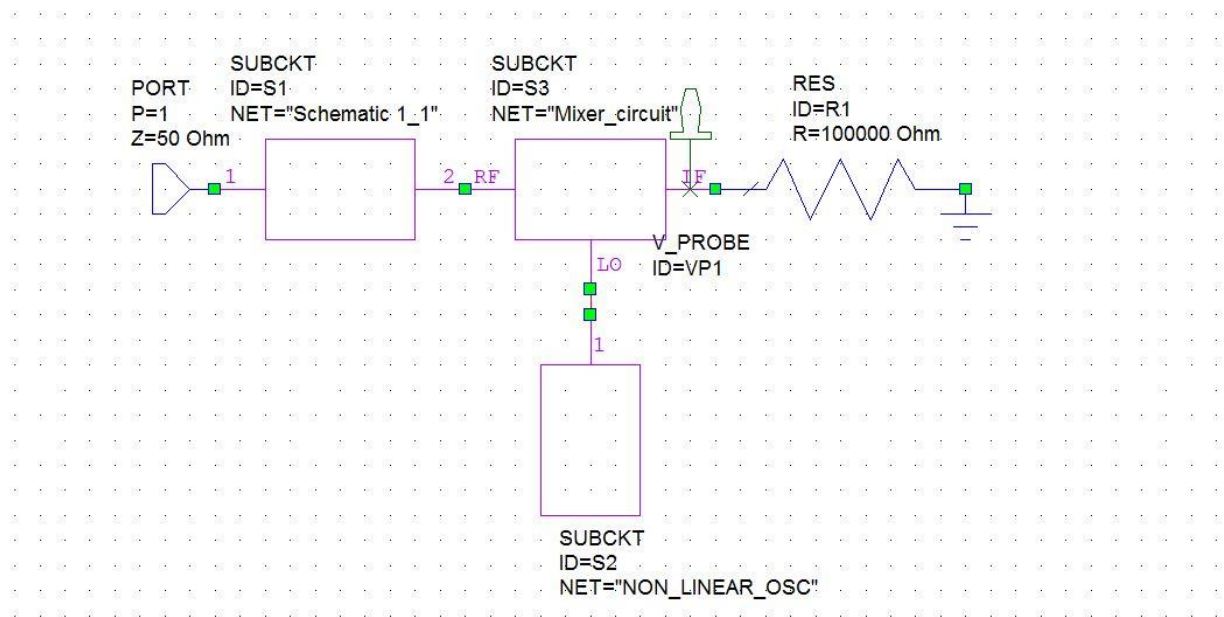
CHAPTER 4: RESULTS

The combined diagram showing all the three components:

1. Low Noise Amplifier
2. Mixer circuit
3. Oscillator circuit.

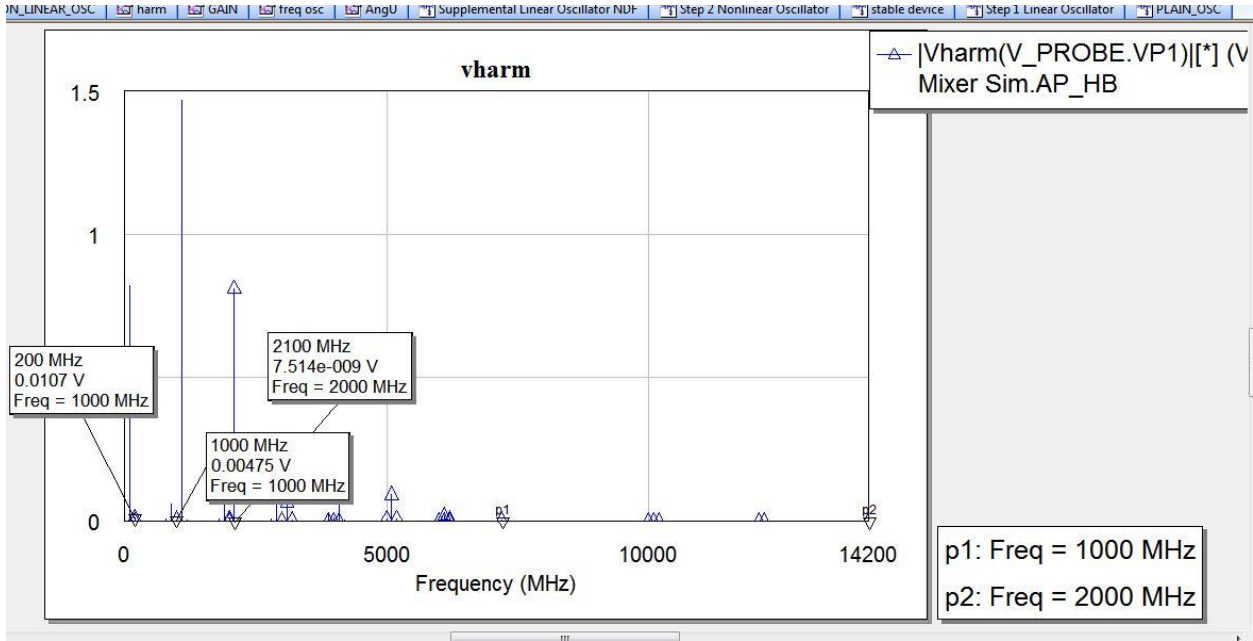
The AWR environment allows us to make them be represented by a unit diagram which has been linked to the actual environment circuit.

This is shown below:



Simulation block diagram

The results obtained from the simulation was obtained as expected. The graph below shows the output from the simulation.



Output graph of the experiment.

The graph shows the upper sideband frequency and the lower sideband frequency.

CHAPTER 5: CONCLUSIONS

The design of the down converter was successfully achieved in the AWR environment. The design of the three components was a complex and time consuming task which allowed me to apply the theory of microwave components and its general principles such as wave reflection, transmission line theory among other topics.

It is from this project that I finally got to truly understand the design process of microwave circuits. The process of choosing the appropriate transistor for a given frequency using the data sheets of its S-parameters and the noise levels data. The project exposed me to the very best industry standard environment AWR. The knowledge of how to use the environment will forever be in my tool set; thanks to the project supervisor, **Mr. Ombura** who made it possible through his advice and the challenges he presented to me.

The experience gained in the design process is worth a lifetime to the designer.

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